A 224-Gb/s Si-Photonic WDM Transmitter with Code-Based Calibration for Simultaneous OMA Locking and RLM Optimization

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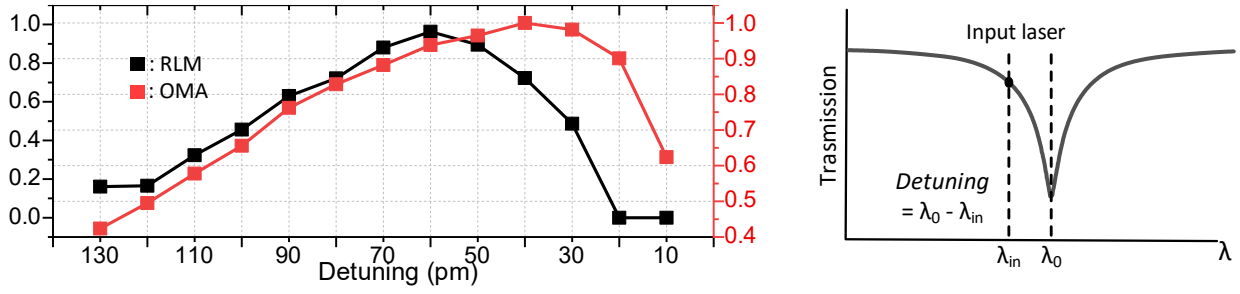
Abstract: This paper demonstrates a Si photonic WDM transmitter using four cascaded microring modulators (MRMs) with co-integrated driver ICs. An on-chip code-based calibration simultaneously locks OMA and optimizes RLM through heater tuning and driver adaptation. The automated scheme enables stable 224-Gb/s operation without external DSP or FPGA.

1. Introduction

Microring modulators (MRMs) are considered key devices for high-density optical interconnects due to their compact footprint, low power consumption, and natural compatibility with wavelength-division multiplexing (WDM). However, their resonant characteristics make them highly sensitive to temperature variations, requiring precise control to ensure stable operation. A code-based calibration technique for maximizing the optical modulation amplitude (OMA) of MRMs has been previously demonstrated [1]. While this approach successfully determines and maintains the MRM temperature that provides the maximum OMA, this condition does not align with the optimal level separation mismatch ratio (RLM) in PAM-4 modulation, as can be seen in Fig. 1(a) in which the normalized measured OMA and RLM for a MRM used in our investigation are shown as a function of the detuning. The detuning is defined as the difference between the MRM resonance wavelength (λ_o) and the input laser wavelength (λ_{in}) as shown in Fig. 1(b). Several approaches have been reported to address this trade-off. In [2], a thermal controller was introduced to identify optimal detuning for a single metric such as extinction ratio, OMA, or RLM, while [3] presented driver adaptation techniques to improve RLM but without an automated control scheme. Neither approach provides a controller that can simultaneously maximize OMA and RLM. In this work, we propose a new code-based dual-objective calibration technique that searches and locks the maximum OMA while adaptively tuning MRM driver strength to optimize RLM. We achieve 224-Gb/s operation with high modulation efficiency and signal linearity across four WDM channels.



(a) (b)

Fig. 1. (a) Measured dependence of normalized OMA and RLM on wavelength detuning in the AMF 220-nm microring modulator at 56-Gb/s. (b) Definition of wavelength detuning ($D = \lambda_o - \lambda_{in}$) between the MRM resonance and input laser.

2. Block Diagram and Controller Logic

Fig. 2(a) shows the architecture of the proposed 224-Gb/s four-channel WDM transmitter. The system integrates a photonic integrated circuit (PIC) that contains four cascaded MRMs with a co-packaged electronic IC (EIC). The EIC integrates a pattern generator that selectively produces PRBS and dedicated calibration code sequences, serializers, a clock distribution network, monitoring circuits, and the calibration controller. The calibration operates in two steps. First, OMA is maximized by a code-based heater search that monitors the average optical levels from integrated photodetectors. Once the heater code corresponding to the OMA peak is identified, it is locked to

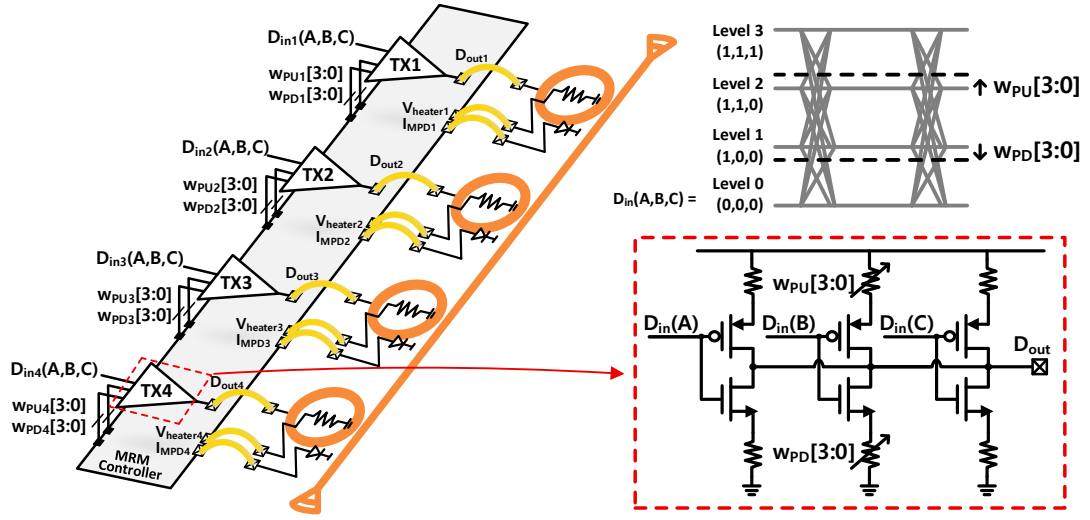
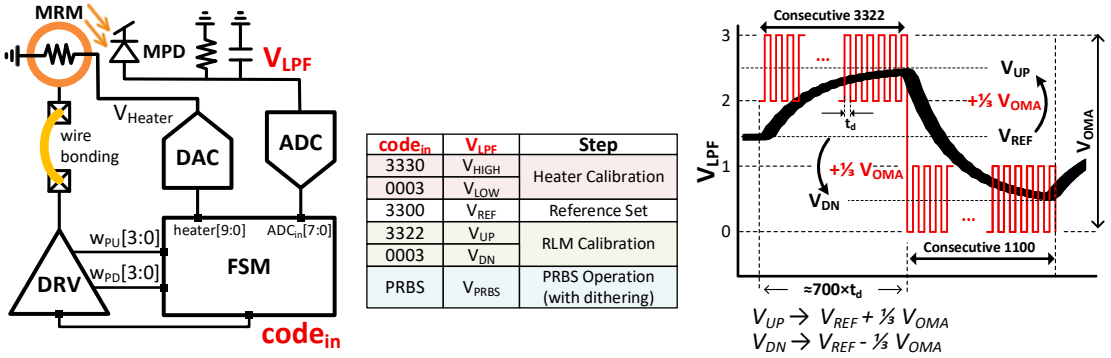


Fig. 2. Block diagram of 4-ch WDM transmitter with driver strength-based RLM control.



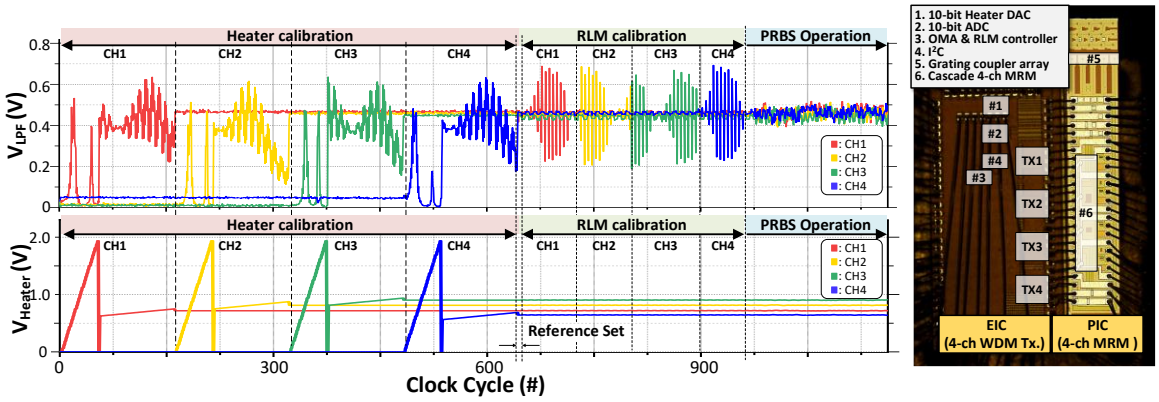
(a) (b)

Fig. 3. (a) Controller block diagram and calibration flow and (b) Relations among LPF output voltages (V_{LPF}) for RLM calibration.

maintain resonance alignment under temperature variations [1]. Second, RLM is optimized through driver adaptation. The MSB and LSB are first converted by thermometer encoding into three bits A, B, and C, such that only a single bit transition occurs between adjacent PAM-4 levels. Here, the B bit directly corresponds to the middle PAM-4 levels, and the driver branch associated with bit B determines levels 1 and 2. The pull-up and pull-down weights w_{PU} and w_{PD} of this branch adjust the absolute positions of levels 1 and 2 independently, where increasing w_{PU} raises level 2, while increasing w_{PD} lowers level 1. The controller sweeps these weights and selects the optimum setting using feedback that monitors the output levels with predefined code patterns and adaptively adjusts w_{PU} and w_{PD} to equalize the intermediate PAM-4 levels, as shown in Fig. 3. Fig. 3(a) shows the controller block diagram, where an on-chip FSM coordinates the heater DAC, ADC, and driver weights. The accompanying table summarizes the input codes and corresponding calibration steps. After the OMA peak is located, V_{OMA} and V_{REF} are obtained and used as references for level calibration, where V_{OMA} is derived from the difference in V_{LPF} values measured with the 3330 and 0003 codes, and V_{REF} is obtained from the V_{LPF} values measured with the 3300 code as the heater-locking reference [1]. Fig. 3(b) illustrates the voltage relations that must hold when the RLM equals 1, where V_{UP} and V_{DN} are positioned at $\pm\frac{1}{3}V_{OMA}$ from V_{REF}. The controller obtains V_{UP} and V_{DN} by repeatedly applying the 3322 and 1100 patterns and measuring the corresponding V_{LPF} values. If the measured difference between V_{UP} and V_{REF} exceeds one-third of V_{OMA}, level 2 is higher than ideal and w_{PU} is decreased. Otherwise, w_{PU} is increased. Similarly, if the difference between V_{REF} and V_{DN} exceeds one-third of V_{OMA}, level 1 is too low and w_{PD} is reduced. Otherwise, w_{PD} is increased. The controller iteratively adjusts w_{PU} and w_{PD} until both conditions are satisfied, achieving that levels 1 and 2 are correctly positioned.

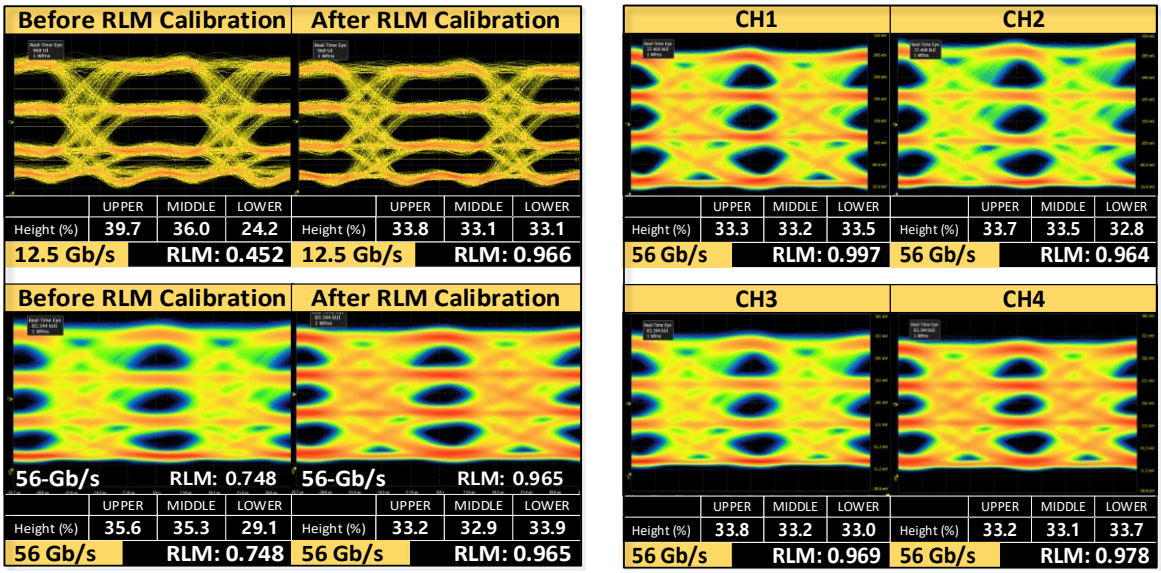
3. Measurement Results

Fig. 4 shows (a) the measured low-pass filtered monitor voltage V_{LPF} and heater bias V_{Heater} during calibration, and (b) the chip micrograph of the co-integrated EIC and PIC. Each channel undergoes heater tuning to maximize



(a) (b)

Fig. 4. (a) Measured LPF output voltage (V_{LPF}) and heater voltage (V_{Heater}) during calibration sequence. (b) Chip micrograph of EIC and PIC.



(a) (b)

Fig. 5. Measured PAM-4 eye diagrams: (a) With and without RLM calibration at 12.5 and 56 Gb/s.
(b) With RLM calibration, 56 Gb/s operation across four WDM channels.

OMA, followed by a reference set step, and then RLM calibration. After calibration, the transmitter enters PRBS operation with dithering enabled. The traces confirm that the proposed on-chip controller automatically identifies the optimum heater points and maintains stable operation across all four channels. Figure 5(a) summarizes RLM calibration at 12.5 Gb/s and 56 Gb/s. We also include 12.5 Gb/s eye diagram to provide bandwidth headroom to assess RLM more clearly without bandwidth-limited ISI. At the maximum OMA point, the PAM-4 eyes still exhibit severe level imbalance (RLM 0.452 at 12.5 Gb/s and 0.748 at 56 Gb/s). After the proposed calibration, the eye openings become balanced and RLM improves to 0.966 and 0.965, respectively, showing that the on-chip controller automatically restores proper level spacing across data rates. Figure 5(b) shows eye diagrams measured across all four WDM channels at 56 Gb/s per channel. The results confirm uniform performance and balanced levels across channels, achieving an aggregate throughput of 224 Gb/s. To our knowledge, this is the first experimental demonstration of an on-chip controller that simultaneously locks OMA and optimizes RLM. Unlike external DSP or FPGA solutions, which are typically area-intensive and introduce significant latency, the proposed scheme enables fully automated calibration in a simple, compact, and energy-efficient design suitable for co-packaged optics (CPO).

4. References

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